General Remarks

Applicant has previously responded to a request similar to that of paragraph 3 of the Office Action in its response filed December 2, 1998. The status of the related applications and patents has not changed since then.

§102 Rejection of the Claims

Claims 1-9, 33-35, 46, and 48-50 were rejected under 35 USC § 102(e) as being anticipated by Manning (U.S. Patent No. 5,610,864). Applicant traverses the rejection, and submits that the Manning reference does not disclose each and every element of the claims. As such, the claims are believed allowable.

Claim 1 recites "mode circuitry configured to select between a burst mode and a pipelined mode" and "circuitry operable in either a burst mode or a pipelined mode ... and configured to switch between the pipelined mode and the burst mode ..." The Office Action does not state where it finds mention in Manning of mode selection circuitry and circuitry coupled to the mode selection circuitry configured to switch between pipelined and burst modes. The only discussion of any such circuitry in the Office Action is a statement that Manning at col. 6, lines 14-16 discloses mode selection circuitry and circuitry coupled to the mode selection circuitry operable to switch between a pipelined and a burst mode of operation. A reading of Manning at col. 6, lines 14-16 reveals something entirely different. The only discussion in Manning of changing modes at col. 6, lines 14-16 is general at best. The statement in Manning is that the Figure 1 memory device "may include the option of switching between burst EDO and standard EDO modes of operation." No circuitry operable in a burst mode or a pipeline mode is present in Manning.

Figure 11 of the present application shown mode circuitry 138. This mode circuitry is configured to select between a burst mode and a pipeline mode of operation as is recited in the claims. No such mode circuitry exists in Manning. See page 27, line 22 to page 29, line 3 for a discussion of the mode circuitry.

The Office Action relies on Manning at Figure 1, ref. 40, col. 6, lines 14-16 and col. 5, lines 43-50 for its rejection of claim 1. Manning does briefly discuss switching between burst EDO and standard EDO modes of operation. However, only a general discussion is present. In Manning, at col. 6, lines 16-22, an initial choice of whether the mode of operation of Manning will be burst EDO or standard EDO is made. The only substantive discussion of any switching occurs at col. 6, lines 30-34: "[I]n a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes."

Reference 40 of Figure 1 is a "mode register which latches the state of one or more of the address input signals ..." Applicant is unable to find any reference in Manning of any circuitry operable in either a burst or pipeline mode. The only support for a pipeline mode in Manning is not for a pipeline mode, but instead for a pipeline architecture. This mention of a pipeline architecture does not teach operation of the Manning memory device in either a pipeline or burst mode, and certainly does not teach switching between a burst mode and a pipeline mode of operation. Manning further does not teach any circuitry for switching between pipeline and burst modes of operation, as is required by claim 1. The mode register 40 of Manning is asserted by the Office Action to be both "mode circuitry configured to select between a burst mode and a pipelined mode" and "circuitry operable in either a burst mode or a pipelined mode ... and configured to switch between the pipelined mode and the burst mode ..." Manning is utterly lacking in any support for that assertion.

Manning does not contain each and every element of claim 1. As such, the rejection of claim 1 is improper. Applicant respectfully requests reconsideration and allowance of claim 1.

Claim 33 recites "selecting between and asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation." Claim 46 recites "selecting a burst mode of operation" and "switching modes to a pipelined mode of operation." Further, claim 46 recites operation in each of the modes. As Applicant has discussed above, nowhere in Manning is any reference to switching between burst and pipeline modes of operation of a memory device.

Instead, the only discussion of any switching is at col. 6, lines 14-34. This discussion clearly contains absolutely no support for switching between burst and pipelined modes of operation as required by the claims.

The methods of claims 33 and 46 each clearly recite switching between burst and pipelined modes of operation in clear contrast to any teaching of Manning. As such, since Manning does not contain each and every element of claims 33 and 46, those claims are allowable.

Claims 2-9, 34-35, and 48-49 depend from and further define patentably distinct claims 1, 33, or 46, and are also believed allowable.

Claim 50 as amended recites a "memory selectively operable either in a burst mode or a pipelined mode." As Applicant has shown above, no teaching of Manning is directed to switching between pipelined and burst modes of operation. As such, Manning does not contain each and every element of claim 50, and it is allowable.

CONCLUSION

Applicant believes the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. The Examiner is invited to telephone the below-signed attorney at (612) 373-6944 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box AF, Assistant Commissioner of Patents, Washington, D.C. 20231 on Aug 30, 1999.

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Name Signature